REMARKS

Claims 1-16, 41-50, and 66-85 are pending in the current application, and claims 1, 6, 9, 13, 41, 44, 47, 66, 71, 76, and 80 have been amended. **If the Examiner does not allow all of the claims after considering this Response, the undersigned requests that the Examiner contact him to schedule and conduct a telephone interview before issuing a subsequent Office Action.**

Rejection Of Claim 1-12, 15-16, 41-46, 49-50, 66, 69-70, 73, 76-77, 80, And 83 Under 35 U.S.C. § 103(a) As Being Unpatentable Over U.S. 7,177,310 to Inagaki In View Of The Examiner's Taking Of Official Notice

Claim 1

Claim 1 as amended recites a hardwired-pipeline circuit operable to process data with an indicated processing pipeline without first generating a virtual address corresponding to the indicated processing pipeline.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [94] – [102] of the patent application, in an embodiment, a hardwired-pipeline circuit 80 is operable to process data with an indicated processing pipeline 74 without first generating a virtual address (see, *e.g.*, paragraph [98]) corresponding to the indicated processing pipeline 74.

In contrast, Inagaki does not teach or suggest processing data with a pipeline without first generating a virtual address corresponding to the pipeline. Referring to FIG. 1 and col. 5, line 66 – col. 6, line 35 of Inagaki, a module 6 includes functional accelerators 11 – 14, which are assigned respective virtual MAC addresses b – e. The module 6 receives an IP packet 134 having a destination IP address 163 (FIG. 3), a unit 105 extracts the destination IP address, and, in response to the extracted IP address, a table 106 provides the virtual MAC address (*e.g.*, address b) of the functional accelerator (*e.g.*, functional accelerator b 11) for processing the data in the IP packet 134. The IP packet 134 (in the form of an Ethernet frame 130) and the virtual MAC address (*e.g.*, address b) are provided to a section 112, which stores the IP packet 134

in the one of the RAMs 150 – 154 (*e.g.*, RAM_b 151) that corresponds to the virtual MAC address (*e.g.*, address b). Subsequently, the module 6 transfers the IP packet 134 from the RAM (*e.g.*, the RAM_b 151) to the one of the function accelerators 11 – 14 (*e.g.*, function accelerator b 11) having the virtual MAC address (*e.g.*, address b) to which the RAM (*e.g.*, the RAM_b 151) corresponds. Consequently, Inagaki's module 6 cannot function as described if it does not generate a virtual MAC address to route the IP packet 134 to the appropriate function accelerator 11 – 14.

Furthermore, the Applicants' attorney disagrees with the following statement on p. 4 of the Office Action: "[h]owever, it should be noted that Inagaki makes not a single mention of executing instructions to perform the claimed steps." But see, *e.g.*, Inagaki's claim 11.

Moreover, the Examiner's reliance on his Official Notice (". . . anything performed in software can be performed solely by hardware and vice-versa") for this and the other rejections in the Office Action is improper because the substance of the Official Notice is conclusion, not fact. Under the Examiner's premise, no apparatus that performs in hardware what was previously performed in software can ever be patentable.

Claims 2-5

These claims are patentable at least by virtue of their dependencies from claim 1.

Claim 6

Claim 6 as amended recites a hardwired-pipeline circuit operable to process data with an identified destination pipeline without first generating a virtual address corresponding to the identified destination pipeline.

In contrast, Inagaki does not teach or suggest processing data with a pipeline without first generating a virtual address corresponding to the pipeline for reasons similar to those discussed above in support of the patentability of claim 1.

Claim 7

Claim 7 recites a hardwired-pipeline circuit operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [51], [57], [82] – [84], and [100] – [104] of the patent application, in an embodiment, a pipeline circuit 80 (FIG. 4) is operable to receive data without receiving information corresponding to the post-processing destination of the data.

In contrast, Inagaki does not teach or suggest a circuit operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data. Referring to FIGS. 1 and 3 and columns 6 and 7, Inagaki's module 6 receives an IP packet 134 that includes a destination IP address 163, which indicates a post-processing destination of the packet (*e.g.*, col. 7, lines 19-32). The destination IP address 163 stays with the packet IP 134 throughout the packet's journey through the module 6 (*e.g.*, col. 7, lines 19-21). If the module 6 did not receive the destination IP address 163 with the IP packet 134, then the module would be unable to route the processed packet 134 to its proper external destination because the module would not "know" where to send the processed packet.

Claims 69-70

These claims are patentable at least by virtue of their dependencies from claim 7.

Claim 8

Claim 8 recites a hardwired-pipeline circuit operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data.

In contrast, Inagaki does not teach or suggest a circuit operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data for reasons similar to those discussed above in support of the patentability of claim 7.

Claim 9

Claim 9 as amended recites an input-data handler operable to load data into a memory without first generating a virtual address corresponding to a specified hardwired pipeline.

In contrast, Inagaki does not teach or suggest an input-data handler operable to load data into a memory without first generating a virtual address corresponding to a specified hardwired pipeline. As discussed above in support of the patentability of claim 1, Inagaki's module 6 does not load data into one of the RAMs 150 – 154 (FIG. 1) without first generating a virtual MAC address corresponding to a function accelerator 11 – 14 specified for processing the data.

Claims 10-12 and 15-16

These claims are patentable at least by virtue of their dependencies from claim 9.

Claim 41

Claim 41 as amended recites processing data with a destination hardwired pipeline circuit without first generating a virtual address corresponding to the destination hardwired pipeline circuit.

In contrast, Inagaki does not teach or suggest processing data with a pipeline circuit without first generating a virtual address corresponding to the pipeline circuit for reasons similar to those discussed above in support of the patentability of claim 1.

Claim 42

This claim is patentable at least by virtue of its dependency from claim 41.

Claim 43

Claim 43 recites receiving data without receiving, with the data, information corresponding to a post processing destination of the data.

In contrast, Inagaki does not teach or suggest a circuit operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data for reasons similar to those recited above in support of the patentability of claim 7.

Claim 83

This claim is patentable at least by virtue of its dependency from claim 43.

Claim 44

Claim 44 as amended recites processing data with a hardwired pipeline without first generating a virtual address corresponding to the hardwired pipeline.

In contrast, Inagaki does not teach or suggest processing data with a pipeline without first generating a virtual address corresponding to the pipeline for reasons similar to those recited above in support of the patentability of claim 1.

Claims 45-46 and 49-50

These claims are patentable at least by virtue of their dependencies from claim 44.

Claim 66

Claim 66 as amended recites a hardwired pipeline circuit operable to generate an identifier, other than a virtual address, that identifies a specified pipeline.

For example, referring, *e.g.*, to FIGS. 4 and 5 and paragraphs [97] - [98] of the patent application, a pipeline circuit 80 is operable to generate an identifier, other than a virtual address, that identifies a specified pipeline 74. The pipeline circuit 80 may receive a message that includes a header and data, and the header may specify the pipeline 74 for processing the data.

In contrast, Inagaki does not disclose or suggest generating an identifier, other than a virtual address, that identifies a specified pipeline. Referring, *e.g.*, to FIG. 1 and col. 6, lines 11-20, Inagaki discloses only that a module 6 generates a virtual MAC

address to identify a function accelerator (*e.g.*, function accelerator b 11) that is specified by a destination IP address 163 for processing data in an IP packet 134.

Claim 73

Claim 73 as amended recites an input data handler operable to load data into a memory without first generating a virtual address corresponding to an indicated hardwired pipeline.

In contrast, Inagaki does not teach or suggest an input data handler operable to load data into a memory without first generating a virtual address corresponding to an indicated hardwired pipeline for reasons similar to those recited above in support of the patentability of claim 9.

Claim 76

Claim 76 as amended recites an input data handler operable to load data into a memory without first generating a virtual address corresponding to an indicated hardwired pipeline.

In contrast, Inagaki does not teach or suggest an input data handler operable to load data into a memory without first generating a virtual address corresponding to an indicated hardwired pipeline for reasons similar to those recited above in support of the patentability of claim 9.

Claim 77

This claim is patentable at least by virtue of its dependency from claim 76.

Claim 80

Claim 80 as amended recites generating an identifier that identifies a hardwired pipeline circuit, the identifier being other than a virtual address.

In contrast, Inagaki does not disclose or suggest generating an identifier that identifies a hardwired pipeline circuit, where the identifier is other than a virtual address, for reasons similar to those recited above in support of the patentability of claim 66.

Rejection Of Claim 13-14, 47-48, 67-68, 71-72, 74-75, 78-79, 81-82, and 84-85 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Inagaki In View Of The Examiner's Taking Of Official Notice And Further In View Of U.S. 4,914,653 To Bishop

Claim 13

Claim 13 recites an input data handler operable to load into an input data queue a pointer to a location of data within a memory, and a pipeline interface operable to retrieve the data from the location using the pointer.

For example, referring, *e.g.*, to FIG. 5 and paragraphs [98] – [100] of the patent application, in an embodiment, an input data handler 20 is operable to load into an input data queue 122 a pointer to a location of data within a memory 100, and a pipeline interface 140 is operable to retrieve the data from the location of the memory 100 using the pointer.

In contrast, in section 39 of the Office Action, the Examiner admits that Inagaki (and inherently admits that his Official Notice) does not disclose an input data handler operable to load into an input data queue a pointer to a location of data within a memory, and an interface operable to retrieve the data from the location using the pointer.

Still in section 39, the Examiner does, however, state that Bishop provides the teaching missing from Inagaki, and thus states that the combination of Inagaki, the Official Notice, and Bishop renders claim 13 obvious.

But as discussed below, Inagaki and Bishop are not combinable to render claim 13 obvious.

It is the Examiner's position that it would have been obvious to modify the module 6 of Inagaki to include an input data queue for holding a pointer as disclosed in Bishop. But the Examiner's position is incorrect.

Referring to FIG. 4, column 2, lines 62-66, and column 7, lines 1-31, Bishop generally teaches using queues and pointers to keep track of multiple groups of data and other information (*e.g.*, packet headers) stored in respective sections of the same memory (see also FIGS. 3 and 5). For example, referring to column 9, lines 48-60, an input queue 143 for a port 202 includes a load pointer 352, which points to the

next data entry 354 in the queue available to be filled with an incoming packet, and includes an unload pointer 353, which points to the last data entry 354 in the queue returned to a user process 140 (FIG. 1).

In contrast, referring to FIG. 1, column 6, line 30 – column 7, line 13, and column 7, lines 33-63, Inagaki discloses the module 6 having separate memories 151-154, separate transmitting buffers 114-117, and separate receiving buffers 120-123, which each correspond to a respective one of the function accelerators 11-14.

Because Inagaki's module 6 includes a separate memory, a separate transmitting buffer, and a separate and receiving buffer for each function accelerator, the module 6 does not need queues that store pointers. In fact, adding such queues to Inagaki's module 6 would at best be redundant, and would increase the complexity of the module 6 with no apparent benefit to offset the increased complexity.

Furthermore, not only would it have been redundant to modify Inagaki's module 6 to include queues that store pointers, but Inagaki teaches away from modifying the module 6 in such a manner. In, *e.g.*, column 7, lines 33-63, and column 8, lines 16-35, Inagaki stresses the importance of maintaining separate memories 151-154, separate transmitting buffers 114-117, and separate receiving buffers 120-123, because this provides advantages that a common memory and common buffers using queues and pointers cannot provide. For example, referring to column 8, lines 30-35, Inagaki states that using separate memories 151-154 and transmitting buffers 114-117 allows these buffers to be clocked at different speeds; this would be difficult, if not impossible, if the memories and transmitting buffers were not separate, but were implemented as different sections of a same memory.

Consequently, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not render claim 13 obvious.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above.

Claims 14, 47-48, 67-68, 71-72, 74-75, 78-79, 81-82, and 84-85

The combination of Inagaki, the Examiner's Official Notice, and Bishop does not render these claims obvious for reasons similar to those recited above in support of the patentability of claim 13.

Conclusion

In view of the foregoing, the application is believed to be in a condition for allowance. The Examiner is encouraged to contact the undersigned via telephone if a conference would expedite prosecution of this matter.

The filing of this document constitutes a request for any needed extension of time. The Commissioner is hereby authorized to charge any deficiency of fees submitted herewith, or credit any overpayment, to Deposit Account No. 07-1897.

Respectfully submitted,

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